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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/831,166	05/07/2001	Sebastien Leveque	034299-329	9044

7590 06/14/2005

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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2638	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/831,166	LEVEQUE ET AL.	
	Examiner	Art Unit	
	Jason M. Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2004*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *1-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 are pending in the instant application.

Claim Objections

2. Claims 1-9 are objected to because of the following informalities:

The following listing of claims 1-9 is presented by the Examiner to correct issues regarding antecedent basis, definite claim language, and typographical errors in the claims.

1. A parallel architecture digital filter receiving p input signals (I_0, ...,I_i,...I_{p-1}) and delivering p output signals (S_0,..., S_i,..., S_{p-1}) which are the sums of the input signals weighted with M coefficients (C_0, C_1,..., C_{M-1}), this filter comprising p parallel channels (V_0,..., V_i,...,V_{p-1}) receiving the input signals (I_0,..., I_i,..., I_{p-1}), characterized in that it comprises r+1 stages (E_0,..., E_j,...,E_r), where r is the integer portion of ratio (M+p-2)/2, the stage of rank j delivering p intermediate signals (R_0^j,...R_i^j,...R_{p-1}^j) which are the weighted sums of the input signals defined by:

~~$$R_i^j = \sum_{q=0}^{p-1} (C_{M-1-q+i-jp}) I_{q+jp}$$~~

$$R_i^j = \sum_{q=0}^{p-1} (C_{M-1-q+i-jp}) I_{q+jp}$$

the filter further comprising a summing means (~~Σ~~) receiving said intermediate signals (R_i^j) and delivering p sums defined by:

$$S_i = \sum_{j=1}^{r} R_i^j$$

these p sums forming p output signals (S_0,...,S_i,...S_{p-1}).

2. The digital filter according to claim 1, wherein the number of channels p is equal to 2, the filter then comprising a first channel with first storing means (R^p) for storing ~~the~~ samples of the input signals of even rank (I_k^p, I_{k-1}^{pi},...) and a second channel

with second storing means (R^i) for storing the samples the input signals of odd rank ($I_k^i, I_{k-1}^i,...$), ~~each channel~~ further comprising first (M_0^p, ..., M_1^p,...ADD^p) and second (M_0^i, ..., M_1^i,...,ADD^i) means ~~respectively~~, for respectively calculating even (S_k^p) and odd (S_k^i) weighted sums~~, respectively~~.

3. The filter according to claim 2, wherein the first and the second means for calculating the even and odd weighted sums each comprise multipliers (M_1^p, M_3^p,..., M_0^i, M_2^i...) each receiving a respective sample of the input signals (I_{k-1}^p, I_k^p,..., I_{k-1}^i, I_k^i...) and a respective weighting coefficient (C_1, C_3, C_0, C_2) (C_0, C_2, C_1,C_3), and an adder (ADD^i, ADD^p) connected to the multipliers.

4. The filter according to ~~claim2~~ claim 3, wherein the first and the second storing means ~~each~~ comprises a first (R^p) and a second (R^i) shift register, respectively.

5. The filter according to claim 4, wherein each shift register (R^p, R^i) comprises cells (B^p) (B^i) arranged in series, each cell consisting of a flip-flop with ~~a~~ an input (D) and a direct output (Q), wherein the input of a flip-flop of rank k is connected to the direct output (Q) of the flip-flop of rank k-1 and the direct output (Q) of ~~a~~ the flip-flop of rank k is connected to the input of the flip-flop of rank k+1, each flip-flop further comprising a complemented output (!Q), each of the multipliers ~~then~~ being a multiplexers (MPX^p) (MPX^i) with two inputs connected to the direct (Q) and complemented (!Q) outputs of the flip-flops, respectively, each ~~multiplier~~ multiplexer further comprising a control input receiving a positive or negative control signal (C_0, C_1,..., C_{m-1}) and an output, which is ~~either~~ connected to a one of the two inputs~~, or to the other,~~ according to the sign of the control signal.

6. A receiver for direct sequence spread spectrum signals comprising:

- ~~at least an analog/digital~~ a digital/analog converter (CAN(I), CAN(Q)) receiving a spread spectrum signal and delivering digital samples of this signal,

-~~at least~~ a digital filter (F(I), F(Q)) with coefficients (C_j) adapted to ~~the~~ a spread spectrum sequence, this filter receiving the digital samples delivered by the digital/analog converter and delivering a filtered signal,

-means (DD, Inf/H, D) for processing the filtered signal ~~able~~ to restore ~~the~~ transmitted data (d), this receiver being characterized in that the digital filter (F(I), F(Q)) is ~~a~~ comprised of parallel architecture digital filters according to any of claims 1 to 5.

7. The receiver according to claim 6, comprising first and second channels in parallel, the first (I) for processing a signal in phase with a carrier and the second (Q) for processing a signal in phase quadrature with said carrier, each channel comprising ~~said~~ a respective parallel architecture digital filter (F(I), F(Q)) with, for the first channel (I), notably, first and second adders ($ADD(I)^p$, $ADD(I)^i$) delivering first and second weighted sums ($S(I)_k^p$, $S(I)_k^i$) and, for the second channel (Q), notably, first and second adders ($ADD(Q)^p$, $ADD(Q)^i$) delivering first and second weighted sums ($S(Q)_k^p$, $S(Q)_k^i$).

8. The receiver according to claim 7, wherein the first channel (I) comprises a first differential demodulation circuit (DD(I)) and the second channel (Q) comprises a second differential demodulation circuit (DD(Q)), the first differential demodulation circuit (DD(I)) receiving the first weighted sums ($S(I)_k^p$, $S(Q)_k^p$) delivered by the respective parallel architecture digital filters (F(I), F(Q)) of the first and second channels (I), (Q), and delivering ~~two~~ a first DOT and a first CROSS signals (DOT^p, $CROSS^p$), the second differential demodulation circuit (DD(Q)) receiving the second weighted sums ($S(I)_k^i$) and ($S(Q)_k^i$) delivered by the respective parallel architecture digital filters (F(I), F(Q)) of the first and second channels (I, Q) and delivering ~~two~~ a second DOT and a second CROSS signals (DOT^i, $CROSS^i$).

9. The receiver according to claim 8, comprising a clock and an information circuit (Inf/H) receiving each of the first and second DOT and CROSS signals (DOT^p, $CROSS^p$), (DOT^i, $CROSS^i$), ~~signals~~ delivered by the first and second differential demodulation circuits (~~DOT~~DD(I), DD(Q)) and delivering ~~two~~ even and odd information signals (S_{inf}^p), S_{inf}^i), a clock signal (SH) and a parity signal (Sp/i).

Appropriate correction is required.

Allowable Subject Matter

3. Claims 1-9 are indicated to contain allowable subject matter for the reasons as applied in the office action dated September 3, 2004.

Conclusion

4. This application is in condition for allowance except for the following formal matters:

The objections above.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
June 10, 2005

jmp

CHIEH M. FAN
PRIMARY EXAMINER